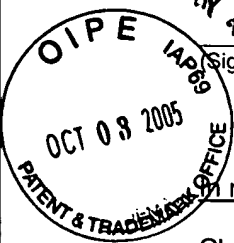


I hereby certify that this correspondence is being deposited via first class mail with the United States Postal Service addressed to : Commissioner of Patents and Trademarks, Alexandria, VA 22313, on September 29, 2005.
The applicant and/or attorney requests the date of deposit as the filing date.

Depositor: ~~Robert Faber~~ Nicole Barrese

IFW



Robert Faber 9-29-05
(Signature & date) Nicole Barrese 9/29/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of _____: September 26, 2005
Cheng, et al. _____: Group Art Unit: 2812
Serial No: 10/710,608 _____: Examiner: Tara Washington
Filed: 7/23/04 _____: International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533

TITLE: Patterned Strained Semiconductor Substrate and Device

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

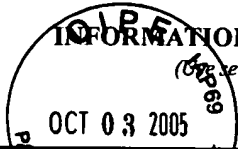
Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the US and non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Cheng, et al.

By Joseph P. Abate 9-26-05
Joseph P. Abate
Registration No. 30,238
Telephone No. 845-894-4633

 <p>INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)</p>	Docket Number (Optional) FIS920040150US1	Application Number 10/710,608
	Applicant(s) Cheng, et al.	
	Filing Date 7/23/04	Group Art Unit 2812

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		3,602,841	8-31-71	McGroddy			
		4,665,415	5-12-87	Esaki, et al.			
		4,853,076	8-1-89	Tsaur, et al.			
		4,855,245	8-8-89	Neppl, et al.			
		4,952,524	8-28-90	Lee, et al.			

U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		US 2001/0009784 A1	7-26-01	Ma, et al.			
		US 2002/0063292 A1	5-30-02	Armstrong, et al.			
		US 2002/0074598 A1	6-20-02	Doyle, et al.			
		US 2002/0086472	7-4-02	Roberds, et al.			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
		JP64-76755	03-1989	Japan				

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si n-MOSFETs". International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
		Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs." 2002 Symposium on VLSI Technology Digest of Technical Papers, IEEE, pp. 98-99.

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

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Application Number

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Applicant(s)

Cheng, et al.

Filing Date

7/23/04

Group Art Unit

2812

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		4,958,213	9-18-90	Eklund, et al.			
		5,006,913	4-9-91	Sugahara, et al.			
		5,060,030	10-22-91	Hoke, et al.			
		5,081,513	1-14-92	Jackson, et al.			
		5,108,843	4-28-92	Ohtaka, et al.			

U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		US 2002/0086497 A1	7-4-02	Kwok			
		US 2002/0090791 A1	7-11-02	Doyle, et al.			
		US 2003/0032261 A1	2-13-03	Yeh, et al.			
		US 2003/0040158 A1	2-27-03	Saitoh			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress." International Electron Devices Meeting, 34.4.1, IEEE, September 1999.

F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Application." International Electron Devices Meeting, 23.5.1, IEEE, April 2000.

EXAMINER

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,134,085	7-28-92	Gilgen, et al.			
		5,310,446	5-10-94	Konishi, et al.			
		5,354,695	10-11-94	Leedy			
		5,371,399	12-6-94	Burroughes, et al.			
		5,391,510	2-21-95	Hsu, et al.			

U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		US 2003/0057184 A1	3-27-03	Yu, et al.			
		US 2003/0067035 A1	4-10-03	Tews, et al.			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design." International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
		A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement." International Electron Devices Meeting, IEEE, March 2001.

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,459,346	10-17-95	Asakawa, et al.			
		5,471,948	12-5-95	Burroughes, et al.			
		5,557,122	9-17-96	Shrivastava, et al.			
		5,561,302	10-1-96	Candelaria			
		5,565,697	10-15-96	Asakawa, et al.			

U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		K. Ota, et al., "Novel Locally Strained Channel Technique for High Performance 55nm CMOS." International Electron Devices Meeting, 2.2.1, IEEE, February 2002.
		G. Zhang, et al., "A New 'Mixed-Mode' Reliability Degradation Mechanism in Advanced Si and SiGe Bipolar Transistors." IEEE Transactions on Electron Devices, vol. 49, no. 12, December 2002, pp. 2151-56.

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*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,571,741	11-5-96	Leedy			
		5,592,007	1-7-97	Leedy			
		5,592,018	1-7-97	Leedy			
		5,670,798	9-23-97	Schetzina			
		5,679,965	10-21-97	Schetzina			

U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		H.S. Momose, et al., "Temperature Dependence of Emitter-Base Reverse Stress Degradation and its Mechanism Analyzed by MOS Structures." Paper 6.2, pp. 140-143.
		C.J. Huang, et al., "Temperature Dependence and Post-Stress Recovery of Hot Electron Degradation Effects in Bipolar Transistors." IEEE 1991 Bipolar Circuits and Technology Meeting 7.5, pp. 170-173.

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,683,934	11-4-97	Candelaria			
		5,840,593	11-24-98	Leedy			
		5,861,651	1-19-99	Brasen, et al.			
		5,880,040	3-9-99	Sun, et al.			
		5,940,716	8-17-99	Jin, et al.			

U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		S.R. Sheng, et al., "Degradation and Recovery of SiGe HBTs Following Radiation and Hot-Carrier Stressing." Pp. 14-15.
		Z. Yang, et al., "Avalanche Current Induced Hot Carrier Degradation in 200 GHz SiGe Heterojunction Bipolar Transistors." Pp. 1-5.

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	Applicant(s) Cheng, et al.	
	Filing Date	Group Art Unit
	7/23/04	2812

U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,940,736	8-17-99	Brady, et al.			
		5,946,559	8-31-99	Leedy			
		5,960,297	9-28-99	Saki			
		5,989,978	11-23-99	Peidous			
		6,008,126	12-28-99	Leedy			

U.S. PATENT APPLICATION PUBLICATIONS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS								
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS		(Including Author, Title, Date, Pertinent Pages, Etc.)
		H. Li, et al., "Design of W-Band VCOs with High Output Power for Potential Application in 77 GHz Automotive Radar Systems." 2003 IEEE GaAs Digest, pp. 263-66.
		H. Wurzer, et al., "Annealing of Degraded npn-Transistors- Mechanisms and Modeling." IEEE Transactions on Electron Devices, vol. 41, no. 4; April 1994, pp. 533-38.

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	Applicant(s) Cheng, et al.	
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7/23/04	2812	

U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,025,280	2-15-00	Brady, et al.			
		6,046,464	4-4-00	Schetzina			
		6,066,545	5-23-00	Doshi, et al.			
		6,090,684	7-18-00	Ishitsuka, et al.			
		6,107,143	8-22-00	Park, et al.			

U.S. PATENT APPLICATION PUBLICATIONS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS								
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS		<i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>
		B. Doyle, et al., "Recovery of Hot-Carrier Damage in Reoxidized Nitrided Oxide MOSFETs." IEEE Electron Device Letters, vol. 13, no. 1, January 1992, pp. 38-40.
		H.S. Momose, et al., "Analysis of the Temperature Dependence of Hot-Carrier-Induced Degradation in Bipolar Transistors for Bi-CMOS." IEEE Transactions on Electron Devices, vol. 41, no. 6, June 1994, pp. 978-987.

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	Applicant(s)	
	Cheng, et al.	
	Filing Date	Group Art Unit
	7/23/04	2812

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,117,722	9-12-00	Wuu, et al.			
		6,133,071	10-17-00	Nagai			
		6,165,383	12-26-00	Chou			
		6,221,735	4-24-01	Manley, et al.			
		6,228,694	5-8-01	Doyle, et al.			

U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

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						YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		M. Khater, et al., "SiGe HBT Technology with Fmax/Ft = 350/300 GHz and Gate Delay Below 3.3 ps". 2004 IEEE, 4 pages.
		J.C. Bean, et al., "GEx Si 1-x/Si Strained-Layer Superlattice Grown by Molecular Beam Epitaxy". J. Vac. Sci. Technol. A 2(2), Apr.-June 1984, pp. 436-440.

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,246,095	6-12-01	Brady, et al.			
		6,255,169	7-3-01	Li, et al.			
		6,261,964	7-17-01	Wu, et al.			
		6,265,317	7-24-01	Chiu, et al.			
		6,274,444	8-14-01	Wang			

U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

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							YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		J.H. Van Der Merwe, "Regular Articles". Journal of Applied Physics, Volume 34, No. 1, January 1963, pp. 117-122.
		J.W. Matthews, et al., "Defects in Epitaxial Multilayers". Journal of Crystal Growth 27 (1974), pp. 118-125.

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Cheng, et al.

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,281,532	8-28-01	Doyle, et al.			
		6,284,623	9-4-01	Zhang, et al.			
		6,284,626	9-4-01	Kim			
		6,319,794	11-20-01	Akatsu, et al.			
		6,361,885	3-26-02	Chou			

U.S. PATENT APPLICATION PUBLICATIONS

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OTHER DOCUMENTS*(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Subramanian S. Iyer, et al., "Heterojunction Bipolar Transistors Using Si-Ge Alloys". IEEE Transactions on Electron Devices, Vol. 36, No. 10, October 1989, pp. 2043-2064.
		R.H.M. Van De Leur, et al., "Critical Thickness for Pseudomorphic Growth of Si/Ge Alloys and Superlattices". J. Appl. Phys. 64 (6), 15 September 1988, pp. 3043-3050.

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U.S. PATENT DOCUMENTS

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		6,362,082	3-26-02	Doyle, et al.			
		6,368,931	4-9-02	Kuhn, et al.			
		6,403,486	6-11-02	Lou			
		6,403,975	6-11-02	Brunner, et al.			
		6,406,973	6-18-02	Lee			

U.S. PATENT APPLICATION PUBLICATIONS

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OTHER DOCUMENTS*(Including Author, Title, Date, Pertinent Pages, Etc.)*

D.C. Houghton, et al., "Equilibrium Critical Thickness for Si 1-x GEx Strained Layers on (100) Si". Appl. Phys. Lett. 56 (5), 29 January 1990, pp. 460-462.

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*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,461,936	10-8-02	von Ehrenwall			
		6,476,462	11-5-02	Shimizu, et al.			
		6,483,171	11-19-02	Forbes, et al.			
		6,493,497	12-10-02	Ramdani, et al.			
		6,498,358	12-24-02	Lach, et al.			

U.S. PATENT APPLICATION PUBLICATIONS

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		6,501,121	12-31-02	Yu, et al.			
		6,506,652	1-14-03	Jan, et al.			
		6,509,618	1-21-03	Jan, et al.			
		6,521,964	2-18-03	Jan, et al.			
		6,531,369	3-11-03	Ozkan, et al.			

U.S. PATENT APPLICATION PUBLICATIONS

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*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,531,740	3-11-03	Bosco, et al.			
		6,621,392	9-16-03	Volant, et al.			
		6,635,506	10-21-03	Volant, et al.			
		6,831,292	12-14-04	Currie, et al.			

U.S. PATENT APPLICATION PUBLICATIONS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

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